ABSTRACT

A method and apparatus for storing and retrieving data in a second, or higher, order prefetch architecture memory integrated circuit. The method includes storing multiple bits of data in memory cells at various electrical distances from an output buffer and retrieving those memory bits concurrently for output. By outputting the bits in a fixed burst order, according to which a bit from a memory cell closer to the output buffer is output before a bit from a memory cell farther from the output buffer, the output time of the data bit from the closer memory cell can be used to mask a portion of the transit time of the bit from the farther memory cell. The apparatus includes memory cells at various locations for storing data bits, an address decoder adapted to store and retrieve multiple bits in a fixed burst order, and a multiplexer.